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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/759,504
Filing Date: January 16, 2004
Appellant(s): MEHTA ET AL.

John F. Conroy

For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed July 9, 2007 appealing from the Office action mailed April 9, 2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,953,020	WANG	9-1999

6,499,072	FRANK	12-2002
6,600,492	SHIMOMURA	4-1999
6,628,292	ASHBURN	9-2003

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 101

Text of sections of Title 35, U.S. Code 101 not included can be found in prior action.

Claims 29-42 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 29-42 are directed to an **article** comprising a **storage** medium which stores computer-executable instructions. Claims to computer-related inventions that are clearly nonstatutory fall into the same general categories as nonstatutory claims in other arts, namely natural phenomena and abstract ideas or laws of nature which constitute "descriptive material." Abstract ideas, or the mere manipulation of abstract ideas, are not patentable. "Functional descriptive material" consists of computer programs which impart functionality when employed as a computer component. Descriptive material is nonstatutory when claimed as descriptive material *per se*. In order for functional descriptive material to be statutory, it must be recorded on some computer-readable medium so that it becomes structurally and functionally interrelated to the medium, since use of technology permits the function of the descriptive material to be realized (*In re Lowry*, 32 F.3d 1579, 1579, 1583-84, 32 USPQ2d 1031, 1035 (Fed. Cir. 1994)). See MPEP 2106 IV B1. The way it is written, Claim 29 appears to be claiming the "article" itself, not the storage medium which stores computer-executable instructions. It is unclear as to

what an "article" is. For example, "article" could be taken to be an entity that is completely separate from computer and simply stores instructions without the computer reading instruction from the entity and executing those instructions. Applicant's disclosure does not define what an "article" is or how an "article" is structurally and functionally interrelated to the computer. Since this claim is directed to a computer-related invention, and could be interpreted in such a way that it is directed to an entity that is completely separate from a computer, it therefore is not structurally and functionally interrelated to the computer, and therefore is non-statutory.

Claim Rejections - 35 USC § 103

Text of sections of Title 35, U.S. Code 103(a) not included can be found in prior action.

1. Claims 1-6, 10-20, 24-34, 38-48, and 52-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang (US005953020A) in view of Frank (US006499072B1).

2. As per Claim 1, Wang teaches method of determining buffer management information for data processing system (c. 3, ll. 47-53) comprising determining buffer drain rate based on first display mode of data processing system (c. 9, ll. 24-31); and calculating one or more buffer management parameters based on at least the buffer drain rate; and making the one or more buffer management parameters available for management of the display buffer (c. 5, ll. 58-61).

However, Wang does not teach determining a latency parameter based on a first system configuration of the data processing system, the latency parameter representing a latency time amount between a display data request and delivery of display data to a display buffer; and calculating one or more buffer management parameters based on at least the latency parameter. However, Frank describes "the adjustable delay to variably control the rate at which data is obtained for a memory request" (c. 4, ll. 11-13), "the issue delay data 24 represents an additional

time delay before starting a memory cycle, **this results in a delay of the returned data by the same amount of time**" (c. 4, ll. 31-35), "The data issue delay data 24 indicates, for example, the amount of delay that the sequencer 20 needs to provide for adjusting data read commands over regulated channels 26a and 26b **from the frame buffer 22 to allow all of the data** from the unregulated bus **to be transferred over the memory read backbone 25**. As such, the adjustable delay sequencer 20 adjusts data command flow over the regulated bus 26a and 26b in response to the data issue delay data to avoid data collision between data **returned from the frame buffer memory 22** and data returned from FIFO buffer 12" (c. 3, ll. 9-17), "the frame buffer is coupled to the multiplexer 48 through one or more read backbone buses 52a and 52b. These datapaths may also include FIFO buffers" (c. 3, ll. 64-67). Therefore, even though the issue delay data 24 represents an artificial delay imposed before the issuance of the read command, this delay in the issuance of the read command also controls the delay of the data between the issuance of the read command (display data request) and the return of data from the frame buffer 22 (delivery of display data) to the memory read backbone FIFO buffers 52a and 52b (display buffer). The delay is determined so that data collisions do not occur over the memory read backbone (c. 2, ll. 54-56). Collisions occur as a result of the amount of data delivered by the parallel access to system and local memory exceeding the data throughput capacity of the buses providing the data transport from the memory controller to the clients (c. 1, ll. 32-41), and this is considered to be a system configuration. Therefore, since the issue delay data 24 is determined, and the issue delay data 24 also controls the delay of the data between the issuance of the read command and the return of data from the frame buffer 22 to the memory read backbone FIFO buffers 52a and 52b, Frank is considered to teach determining a latency

parameter (issue delay data 24) based on a first system configuration of the data processing system, the latency parameter representing a latency time amount between a display data request (issuance of the read command) and delivery of display data to a display buffer (memory read backbone FIFO buffers 52a and 52b); and calculating one or more buffer management parameters based on at least the latency parameter (c. 3, ll. 7-17).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Wang to include determining a latency parameter based on a first system configuration of the data processing system, the latency parameter representing a latency time amount between a display data request and delivery of display data to a display buffer; and calculating one or more buffer management parameters based on at least the latency parameter as suggested by Frank because Frank suggests that the buffer management parameter must be based on the latency parameter in order to avoid collisions from occurring which create an efficiency problem and potential data throughput bottlenecks (c. 2, ll. 54-56; c. 1, ll. 32-41).

3. As per Claim 2, Wang describes determining a buffer fill rate based on a buffer configuration (c. 8, ll. 3-8; c. 9, ll. 26-31); and calculating at least one of the one or more buffer management parameters based on the buffer fill rate (c. 5, ll. 1-3).

4. As per Claim 3, Wang describes calculating at least one of the one or more buffer management parameters based on a buffer size (c. 4, ll. 22-28; c. 4, ll. 38-42).

5. As per Claim 4, Wang describes that the one or more buffer management parameters comprise a watermark level (c. 6, ll. 14-17).

6. As per Claim 5, Wang describes that the watermark level comprises a lower bound of a desired watermark level range (*low watermark threshold value*, c. 9, ll. 17-23).

7. As per Claim 6, Wang describes that the watermark level comprises an upper bound of a desired watermark level range (*high watermark*, c. 9, ll. 10-16).

8. As per Claim 10, Wang describes detecting a change from the first display mode to a second display mode; and calculating at least one of the one or more buffer management parameters based on the second display mode (c. 8, ll. 44-50).

9. As per Claim 11, Wang describes detecting a change from the first system configuration to a second system configuration (c. 5, ll. 53-57); and calculating at least one of the one or more buffer management parameters based on the second system configuration (c. 6, ll. 7-13).

10. As per Claim 12, Wang does not teach latency parameter represents maximum expected latency time amount for first system configuration of data processing system. However, Frank teaches issue delay data 24 also controls delay of data between issuance of read command (display data request) and return of data from the frame buffer 22 (delivery of display data) to the memory read backbone FIFO buffers 52a and 52b (display buffer), as discussed in the rejection for Claim 1, and therefore Frank teaches maximum amount of time including the sum of the issue delay data 24 and the latency time between a display data request (issuance of the read command) and delivery of display data (return of data from the frame buffer 22 to the memory read backbone FIFO buffers 52a and 52b). The delay is determined according to the threshold of the buffer to ensure that the buffer does not overflow (c. 4, ll. 63-c. 5, ll. 17; c. 2, ll. 47-51). The delay is determined so that data collisions do not occur over the memory read backbone (c. 2, ll. 54-56). Collisions occur as a result of the amount of data delivered by the parallel access to system and local memory exceeding the data throughput capacity of the buses providing the data transport from the memory controller to the clients (c. 1, ll. 32-41), and this is considered to be a

system configuration. Therefore, the latency parameter represents a maximum expected latency time amount for the first system configuration of the data processing system. This would be obvious for the same reasons given in the rejection for Claim 1.

11. As per Claim 13, Wang teaches first display mode is characterized by of first refresh rate (c. 4, ll. 16-18), first display resolution (c. 5, ll. 53-57), first color depth (c. 10, ll. 19-21).

12. As per Claim 14, Wang does not teach that the first system configuration is characterized at least by a buffer memory type. However, Frank discloses that the first system configuration is characterized at least by a buffer memory type (c. 1, ll. 32-39).

It would have been obvious to one ordinary skill in the art at the time of invention by applicant to modify device of Wang so first system configuration is characterized by buffer memory type because Frank suggests apparatus needs to know what type of memory the memory request is being made to in order to determine whether delay is necessary (c. 5, ll. 17-40).

13. As per Claim 15, Wang teaches display part (14, Fig. 1) which directs movement of display data, display part including buffer (30) to store display data to be displayed on display screen (40) (c. 4, ll. 2-16); and data computing system configured to calculate one or more buffer management parameters based on buffer drain rate based on first display mode; wherein buffer drain rate represents rate at which display data is read from buffer (c. 9, ll. 26-31; c. 5, ll. 58-61).

However, Wang does not teach calculating one or more buffer management parameters based on latency parameter based on a first system configuration; wherein the latency parameter represents a latency time amount between a display data request and delivery of display data to the buffer. However, Frank teaches this limitation, as discussed in the rejection for Claim 1.

14. As per Claims 16-20 and 24-28, these claims are similar in scope to Claims 2-6 and 10-14 respectively, and therefore are rejected under the same rationale.

15. As per Claim 29, Claim 29 is similar in scope to Claim 1, except that Claim 29 is for an article comprising a storage medium which stores computer-executable instructions, the instructions being readable and operable to cause a computer to perform the method of Claim 1. Wang describes an article comprising a storage medium which stores computer-executable instructions, the instructions being readable and operable to cause a computer to perform the method (c. 5, ll. 26-39). Therefore, Claim 29 is rejected under the same rationale as Claim 1.

16. As per Claims 30-34, 38-48, 52-56, these claims are similar in scope to Claims 2-6, 10-20, and 24-28 respectively, and therefore are rejected under the same rationale.

17. As per Claim 57, Wang teaches determining buffer management information for data processing system (c. 3, ll. 47-53), comprising determining drain rate at which data to be drained from display FIFO buffer memory based on display mode supported by graphics processor (c. 9, ll. 24-31); calculating watermark value based on at least drain rate; and making watermark value available for management of display FIFO buffer memory (c. 6, ll. 5-22; c. 9, ll. 10-23).

However, Wang does not teach determining maximum amount of time that access to local memory to obtain data to supply a display FIFO buffer memory may be delayed and calculating watermark value based on at least maximum amount of time. However, Frank teaches issue delay data 24 also controls delay of data between issuance of read command (display data request) and return of data from the frame buffer 22 (delivery of display data) to memory read backbone FIFO buffers 52a and 52b (display buffer), as discussed in rejection for Claim 1, and so Frank teaches maximum amount of time including sum of issue delay data 24

and latency time between a display data request (issuance of the read command) and delivery of display data (return of data from the frame buffer 22 to the memory read backbone FIFO buffers 52a and 52b). Therefore, Frank discloses determining the maximum amount of time that access to a local memory (22, Fig. 1) to obtain data to supply a display FIFO buffer memory (52) may be delayed (c. 4, ll. 11-13, 53-62; c. 3, ll. 64-67). The delay is determined so that data collisions do not occur over the memory read backbone (c. 2, ll. 54-56). Frank discloses calculating a watermark value (28, Fig. 1) based on at least the maximum amount of time (c. 3, ll. 22-29; c. 4, ll. 63-c. 5, ll. 17). This would be obvious for the same reasons given in the rejection for Claim 1.

18. Claims 7, 9, 21, 23, 35, 37, 49 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang (US005953020A) and Frank (US006499072B1) in view of Shimomura (US006600492B1).

19. As per Claim 7, Wang and Frank are relied upon for teachings relative to Claim 1.

However, Wang and Frank do not teach that the one or more buffer management parameters comprise a burst length. However, Shimomura describes that the one or more buffer management parameters (c. 16, ll. 27-37) comprise a burst length (c. 21, ll. 4-23).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the devices of Wang and Frank so that the one or more buffer management parameters comprise a burst length as suggested by Shimomura because Shimomura suggests that adjusting the burst length can reduce the amount of power consumption (c. 21, ll. 6-11).

20. As per Claim 9, Wang does not teach that the burst length comprises an upper bound of a desired burst length range. However, Shimomura describes that the burst length comprises an upper bound of a desired burst length range (c. 21, ll. 12-23, c. 21, ll. 33-40).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Wang so that the burst length comprises an upper bound of a desired burst length range as suggested by Shimomura because Shimomura suggests that the larger the burst length, the more the power consumption is reduced (c. 21, ll. 6-11), and therefore the system needs to know the upper bound of the desired burst length range.

21. As per Claims 21 and 23, these claims are similar in scope to Claims 7 and 9 respectively, and so are rejected under same rationale. As per Claims 35 and 37, these claims are similar in scope to Claims 7 and 9 respectively, and so are rejected under same rationale. As per Claims 49 and 51, these claims are similar in scope to Claims 21 and 23 respectively, and so are rejected under same rationale.

22. Claims 8, 22, 36, and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang (US005953020A), Frank (US006499072B1), and Shimomura (US006600492B1) in view of Ashburn (US006628292B1).

23. As per Claim 8, Wang, Frank, and Shimomura are relied on for teachings for Claim 7.

However, Wang, Frank, and Shimomura do not teach that the burst length comprises a lower bound of a desired burst length range. However, Ashburn describes that the burst length comprises a lower bound of a desired burst length range (c. 2, ll. 35-46).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the devices of Wang, Frank, and Shimomura so that the burst length comprises a lower bound of a desired burst length range as suggested by Ashburn because Ashburn suggests that the system needs to know the minimum burst length that can create a free command cycle in order to increase memory bandwidth (c. 2, ll. 24-27, 36-38).

24. As per Claims 22 and 36, these claims are both similar in scope to Claim 8, and so are rejected under same rationale. As per Claim 50, it is similar in scope to Claim 22, and so is rejected under same rationale.

Allowable Subject Matter

25. Claims 60-62 are allowed.

26. Claims 58-59 are objected to as being dependent on rejected base claim, but would be allowable if written in independent form including all limitations of base and intervening claims.

(10) Response to Argument

1. Applicant's arguments, see pages 8-9, filed July 9, 2007, with respect to the 35 U.S.C. 101 rejections of Claims 1-14 and 57-62 have been fully considered and are persuasive. The 35 U.S.C. 101 rejections of Claims 1-14 and 57-62 have been withdrawn.

2. Applicant's arguments filed July 9, 2007, with respect to the 35 U.S.C. 101 rejections of Claims 29-42 and the 35 U.S.C. 103(a) rejections have been considered but are not persuasive.

3. Applicant argues that 35 U.S.C. 101 does not preclude entities that are "completely separate from a computer" from patentability (page 10).

In reply, the Examiner points out that this claim is directed to a computer-related invention, and the MPEP recites that **claims to computer-related inventions** that are clearly nonstatutory include descriptive material that is nonstatutory when claimed as descriptive material per se. In order for functional descriptive material to be statutory, **it must be structurally and functionally interrelated to the computer**, since use of technology permits the function of the descriptive material to be realized (*In re Lowry*, 32 F.3d 1579, 1579, 1583-84, 32 USPQ2d 1031, 1035 (Fed. Cir. 1994)). See MPEP 2106.01. Since this claim is directed to a

computer-related invention, and could be interpreted in such a way that it is directed to an entity that is completely separate from a computer, it therefore is not structurally and functionally interrelated to the computer, and therefore is non-statutory.

4. Applicant argues that there is no requirement that a computer read a computer program encoded on a computer-readable medium set forth in the MPEP. Instead, a computer-readable medium encoded with a computer program defines structural and functional interrelationships and hence constitutes patentable subject matter (page 11).

In reply, the Examiner points out MPEP sets forth that in order for functional descriptive material to be statutory, it must be structurally and functionally interrelated to the computer (MPEP 2106.01). The way it is written, Claim 29 appears to be claiming the "article" itself, not the storage medium which stores computer-executable instructions. It is unclear as to what an "article" is. For example, "article" could be taken to be an entity that is completely separate from a computer and simply stores instructions without the computer reading the instruction from the entity and executing those instructions. Applicant's disclosure does not define what an "article" is or how an "article" is structurally and functionally interrelated to the computer. So, there is no clear structural and functional interrelationship between the "article" and the computer.

5. Applicant argues that Frank's (US006499072B1) data issue delay data 24 represents an artificial delay imposed before the issuance of a read command to constitute a time between issuance of a display data request and delivery of display data. A delay before the issuance of a data read command is prior to the issuance of a data read command, rather than "between a display data request and delivery of display data to a display buffer" (pages 12-14).

In reply, the Examiner points out Frank describes "the adjustable delay to variably control the rate at which data is obtained for a memory request" (c. 4, ll. 11-13); "the issue delay data 24 represents an additional time delay before starting a memory cycle, **this results in a delay of the returned data by the same amount of time**" (c. 4, ll. 31-35), "The data issue delay data 24 indicates, for example, the amount of delay that the sequencer 20 needs to provide for adjusting data read commands over regulated channels 26a and 26b **from the frame buffer 22 to allow all of the data** from the unregulated bus **to be transferred over the memory read backbone 25**. As such, the adjustable delay sequencer 20 adjusts data command flow over the regulated bus 26a and 26b in response to the data issue delay data to avoid data collision between data **returned from the frame buffer memory 22** and data returned from FIFO buffer 12" (c. 3, ll. 9-17), "the frame buffer is coupled to the multiplexer 48 through one or more read backbone buses 52a and 52b. These datapaths may also include FIFO buffers" (c. 3, ll. 64-67). Therefore, even though the issue delay data 24 represents an artificial delay imposed before the issuance of the read command, this delay in the issuance of the read command also controls the delay of the data between the issuance of the read command (display data request) and the return of data from the frame buffer 22 (delivery of display data) to the memory read backbone FIFO buffers 52a and 52b (display buffer). Therefore, since issue delay data 24 is determined, and the issue delay data 24 also controls the delay of the data between the issuance of the read command and the return of data from the frame buffer 22 to the memory read backbone FIFO buffers 52a and 52b, Frank is considered to teach determining a latency parameter (issue delay data 24) representing a latency time amount between a display data request (issuance of the read command) and delivery of display data to a display buffer (memory read backbone FIFO buffers 52a and 52b).

6. Applicant argues that Claim 57 recites a maximum amount of time that access to a local memory to obtain data to supply a display FIFO buffer memory may be delayed. Such a maximum amount of time includes the sum of Frank's data issue delay data and any latency time between a display data request and delivery of display data (pages 16-17).

In reply, the Examiner points out Frank teaches issue delay data 24 also controls delay of the data between the issuance of the read command (display data request) and the return of data from the frame buffer 22 (delivery of display data) to the memory read backbone FIFO buffers 52a and 52b (display buffer), as discussed above, and therefore Frank does teach this maximum amount of time including the sum of the issue delay data 24 and the latency time between a display data request (issuance of the read command) and delivery of display data (return of data from the frame buffer 22 to the memory read backbone FIFO buffers 52a and 52b).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Joni Hsu

Conferees:

Kee Tung

Ulka Chauhan